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History.SchDoc

Revision History

Rev.	Rel.	Date	Author	Description	Page(s)
1.1.1	RC00	2021-09-14	RP	- Initial design	
2	RC00	2023-8-9	GLS	Clean Up	
3	RC00	2024-4-22	JH	Finishing touches	

EVAL1_BUP_15N(06N)

EVAL1_BUP_15N

2

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IRHIR PSS HiRel M TM

Andover, Ma

04/2024

Link to Top Level Document

02 Top Level
Top_Level.SchDoc

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Title	EVAL1_BUP_15N(06N)		
Variant	EVAL1_BUP_15N	Approved	<Appr.>
Size: A3	Document Name: History.SchDoc	Rel.: JH	Rev.: 2
Author: Jack Heun			
Date: 8/29/2024 Time: 9:47:15 AM	SVN Revision: Not in version control		
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Top_Level.SchDoc

Schematic
Schematic.SchDoc

Gate Drivers, Half Bridge Power Stage

Miscellaneous
Miscellaneous.SchDoc

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Size: A3	Document Name: Top_Level.SchDoc	Rel.: JH	Rev.: 2

Author: Jack Heun
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Schematic.SchDoc

VIN
150 V (60 V) MAX

X5 282836-2 (+) VIN
X8 282836-2 (-)
C1 100uF
X11 5010
X12 5011
PGND

C2 1uF
C3 1uF
C4 100nF
C5 100nF
C6 100nF
C7 10nF
C8 10nF
Close to Q1 Drain

VDD
C19 1uF
C20 100nF
PGND

Internal Bootstrap Diode
Vcc to VB

VSW

J1 H1 22-28-4023
SMA1 SMA-J-P-H-RA-TH1
PWM_IN / PWM_HIN
PWM Input 0V to 5V
SGND
X1 IN / HIN
X15 5012
IN / HIN
SGND
R5 50R
SGND

C10 100nF (DNP)
R4 DNP
C12 100nF
R1 100k
J3 X17 22-28-4033

J2 H2 22-28-4023
SMA2 SMA-J-P-H-RA-TH1
SD / PWM_LIN
PWM Input 0V to 5V
SGND
X2 SD / LIN
X16 5012
SD / LIN
SGND
R6 DNP
SGND

U1 2ED21844S06J
VCC, VSS, VB, HO, VS, IN, DT, SD_N, LO, COM, NC1, NC2, NC3, NC4

Rg1 4.99 ohm
Vg_Q1
D1 30V 10A
Rg2 0R
Q1
Cboot 2.2uF 25V
RVS 0R
X13 VG1
PGND

Rg3 4.99 ohm
Vg_Q2
D2 30V 10A
Rg4 0R
Q2
X14 VGS2
PGND
PGND

VSW
X10 VSW
PGND
R3 1.6R
C11 3.3nF
PGND
X9 282836-2
X6 282836-2
PGND

Nominal Dead Time
Range:
400 ns to 3 us

X3 B_Jack1 575-6
VDD
10V to 15V
12V Nominal
5010
C21 100nF
C9 1uF
R2 1k
D3 Green/5V
X7 B_Jack2 575-6
5011
PGND

X4 5011
R8 DNP
PGND
SGND

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Miscellaneous.SchDoc

MP1



9434

MP2



9434

MP3



9434

MP4



9434

Fiducial Markers

E1



E2



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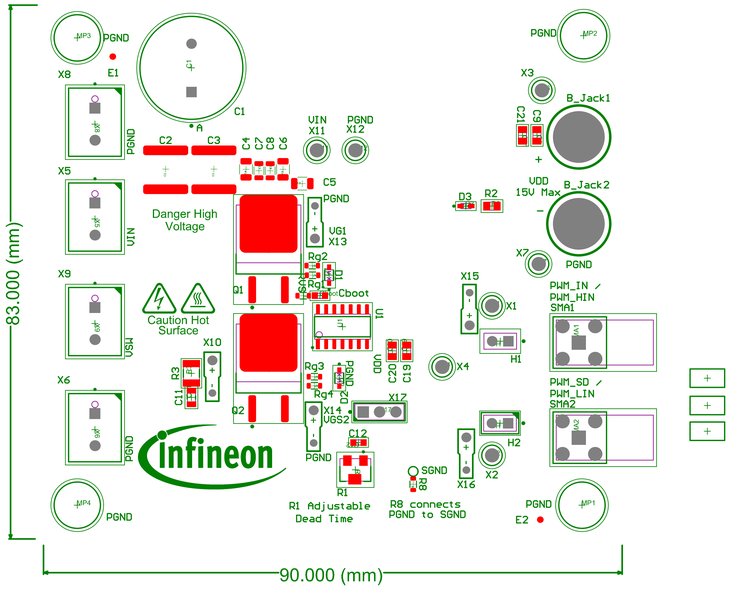
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Layer 1	CF-005	2.76mil		
	Dielectric 1	FR-4	10.00mil	4.2	
2	Layer 2	CF-004	2.76mil		
	Dielectric 2	FR-4	30.18mil	4.2	
3	Layer 3	CF-004	2.76mil		
	Dielectric 3	FR-4	10.00mil	4.2	
4	Layer 4	CF-005	2.76mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Total board thickness: 62.00mil



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.12 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 65 MIL (1.65mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

IOR HiRel
An Infineon Technologies Company

Infineon Technologies AG
IRHR PSS HiRel M TM
101 N Pacific Coast Highway
El Segundo, CA 90245

ENGINEER:	TITLE: EVAL1_BUP_15N(06N)		
PCB DESIGNER: Jack Heun			
DATE: 8/29/2024	PART NO.:	REL: 2	REV: 2
SVN REVISION: Not in version control	FILE NAME: EVAL1_BUP_15N(06N).PcbDoc	APRV: JH	SCALE: 1:1

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	8\29\2024 DATE:	PART NO.:	2 REF:	2 REV:
	Jack Heun PCB DESIGNER:	EVAL1_BUP_1SN(OSN) TITLE:		
	ENGINEER:			